COMPUTER ARCHITECTURE –CS1251

IV- SEMESTER

UNIT I- BASIC STRUCTURE OF COMPUTER

1. What are the basic functional units of a computer?

Ans: A computer consists of five functionally independent main parts namely

- Input Unit
- Memory Unit
- Arithmetic and logic Unit
- Output Unit
- Control Unit

2. Define RAM.

Ans: Memory in which any location can be reached in a short and fixed amount of time after specifying its address is called random access memory.

3. Define memory access time.

Ans: The time required to access one word is called memory access time.

4. What is instruction register (IR) and program counter (PC) used for ?

Ans: The instruction register (IR) holds the instruction that is currently being executed .Its output is available to the control circuits which generate the timing signals that control the various processing elements.

The program counter PC) is used to keep track of the execution of the program. It contains the memory address of the next instruction to be fetched and executed.

5. What do you mean by memory address register(MAR) and memory data register(MDR)?

Ans: The MAR holds the address of the location to be accessed. The MDR contains

6. What is an interrupt?

Ans: An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing an appropriate interrupt service routine.

7. Explain about Bus.

Ans: Bus is a group of lines that serves as a connecting path for several devices. In addition to the lines that carry the data , the bus must have the lines for address and control purposes.

8. What do you mean by multiprogramming or multitasking?

Ans: The operating system manages the concurrent execution of several application programs to make best possible use of computer resources. This pattern of concurrent execution is called multiprogramming or multitasking.

9. Give the basic performance equation.

Ans: The basic performance equation is given as

$$T = N \times S / R$$

T = It is the processor time required to execute a program
N= It is the actual number of instruction executions.
S = It is the average number of basic steps neede to execute one machine instruction.
R = It is the clock rate.

10. Explain the concept of pipelining.

Ans: Pipelining is the means of executing machine instructions concurrently. It is the effective way of organizing concurrent activity in a computer system. It is a process of substantial improvement in the performance by overlapping the execution of successive instructions.

11. What are the two techniques used to increase the clock rate R?

Ans: The two techniques used to increase the clock rate R are:
1. The integrated – circuit (IC) technology can be increased which reduces the time needed to complete a basic step.
2. We can reduce the amount of processing done in one basic step.

12. What is Big – Endian and Little- Endian representations.

Ans: The Big- endian is used when lower byte addresses are used for the more significant bytes (The leftmost bytes) of the word.
The little-endian is used for the opposite ordering, where the lower byte addresses are used for the less significant bytes (the rightmost bytes) of the word.

13. What is addressing mode?

14. What are the different types of addressing modes available?

Ans: The different types of addressing modes available are:

- Immediate addressing mode
- Register addressing mode
- Direct or absolute addressing mode
- Indirect addressing mode
- Indexed addressing mode
- Relative addressing mode
- Autoincrement
- Autodecrement

15. What is indirect addressing mode?
Ans: The effective address of the operand is the contents of a register or memory location whose address appears in the instruction

16. What is indexed addressing mode?
Ans: The effective address of the operand is generated by adding a constant value to the contents of a register.

17. Define autoincrement mode of addressing?
Ans: The effective address of the operand is the contents of a register specified in the instruction. After accessing the operand, the contents of this register are automatically incremented to point to the next item in the list.

18. Define autodecrement mode of addressing?
Ans: The contents of a register specified in the instruction are first automatically decremented and are then used as the effective address of the operand.

19. What are condition code flags? What are the commonly used flags?
Ans:The processor has to keep track of the information about the results of various operations for the subsequent conditional branch instructions. This is done by recording required information in individual bits called condition code flags.
Four commonly used flags are:

- N(Negative)
- Z(Zero)
- V(overflow)
- C(Carry)

20. What do you mean by assembler directives?
Ans: These are the instructions which direct the program to be executed. They have no binary equivalent so they are called pseudo-opcodes. These instructions are used to define symbols, allocate space for variable, generate fixed tables etc.
Examples : END, NAME

21.

program is executed it performs a sequence of input operations needed to transfer the machine language program from the disk into a specified place in the memory.

22. What do you man by relative addressing mode?
Ans: The effective address is determined by the index mode using the program counter in place of the general purpose register R_i**.**

23. What is Stack?
Ans: A stack is a list of data elements, usually words or bytes with the accessing restriction that elements can be added or removed at one end of the list only. It follows last in first out (LIFO) mechanism.

24. What is a queue?

Ans: Is a type of datastructure in which the data are stored in and retrieved on a First in first out(FIFO) basis. It grows in the direction of increasing addresses in the memory. New data are added at the back (High-address end) and retrieved from the front (low-address end) of the queue.

25. What are the difference between Stack and Queue?

STACK	QUEUE
One end of stack is fixed (the bottom) while the other end rises and falls as data are pushed and popped	Both ends of a queue move to higher addresses
Single Pointer is needed to point to the top of the stack	Two pointers are needed to keep track of the two ends of the queue

UNIT II - ARITHMETIC UNIT

1. What is half adder?

Ans: A half adder is a logic circuit with two inputs and two outputs, which adds two bits at a time, producing a sum and a carry.

2. What is full adder?

Ans: A full adder is logic circuit with three inputs and two outputs, which adds three bits at a time giving a sum and a carry.

3. What is signed binary?

Ans: A system in which the leading bit represents the sign and the remaining bits the magnitude of the number is called signed binary. This is also known as sign magnitude.

4. What are the two approaches used to reduce delay in adders?

Ans:1) The first approach is to use the fastest possible electronic technology in

5. What is a carry look-ahead adder?

Ans: The input carry needed by a stage is directly computed from carry signals obtained from all the preceding stages i-1,i-2,…..0, rather than waiting for normal carries to supply slowly from stage to stage. An adder that uses this principle isa called carry look-ahead adder.

6. What are the main features of Booth's algorithm?

Ans: 1) It handles both positive and negative multipliers uniformly.

2) It achieves some efficiency in the number of addition required when the multiplier has a few large blocks of 1s.

7. How can we speed up the multiplication process?

Ans: There are two techniques to speed up the multiplication process:

1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands.

2) The second technique reduces the time needed to add the summands.

8. What is bit pair recoding? Give an example.

Ans: Bit pair recoding halves the maximum number of summands. Group the Booth-recoded multiplier bits in pairs and observe the following: The pair (+1 -1) is equivalent to to the pair (0 +1). That is instead of adding -1 times the multiplicand m at shift position i to +1 × M at position i+1, the same result is obtained by adding +1 × M at position i.

Eg: 11010 – Bit Pair recoding value is 0 -1 -2

9. What are the two methods of achieving the 2's complement?

a. Take the 1's complement of the number and add 1.
b. Leave all least significant 0's and the first unchanged and then complement the remaining bits.

10. What is the advantage of using Booth algorithm?

Ans: 1) It handles both positive and negative multiplier uniformly.

2) It achieves efficiency in the number of additions required when the multiplier has a few large blocks of 1's.

3) The speed gained by skipping 1's depends on the data.

11. Write the algorithm for restoring division.

Ans: Do the following for n times:

1) Shift A and Q left one binary position.

2) Subtract M and A and place the answer back in A.

3) If the sign of A is 1, set q0 to 0 and add M back to A.

Where A- Accumulator, M- Divisor, Q- Dividend.

Step 1: Do the following for n times:

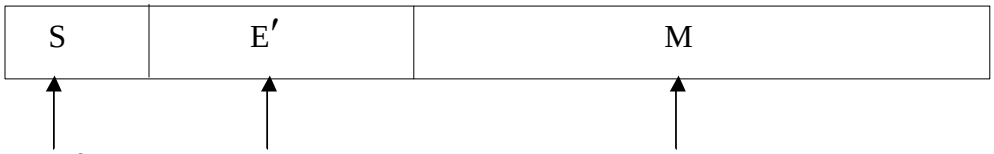
1) If the sign of A is 0 , shift A and Q left one bit position and subtract M from A; otherwise , shift A and Q left and add M to A.

2) Now, if the sign of A is 0,set q0 to 1;otherwise , set q0 to0.

Step 2: if the sign of A is 1, add M to A.

13. Give the IEEE standard for floating point numbers for single precision number.

Ans:



Sign of the Number
0 – Positive
1 - Negative

8-bit signed exponent in excess-127 representations

23- bit Mantissa fraction

value represented= $\pm$ 1. M$\times$ 2^{E-127}

14. Give the IEEE standard for floating point numbers for double precision number.

Ans:

Sign of the Number
0 – Positive
1 - Negative

11-bit signed exponent in excess-1023 representations

52- bit Mantissa fraction

value represented= $\pm$ 1. M$\times$ 2^{E-1023}

15. When can you say that a number is normalized?

Ans: When the decimal point is placed to the right of the first (nonzero) significant digit, the number is said to be normalized.

Ans: The end values 0 to 255 of the excess-127 exponent E are used to represent special values such as:

a) When E′= 0 and the mantissa fraction M is zero the value exact 0 is represented.
b) When E′= 255 and M=0, the value ∞ is represented.
c) When E′= 0 and M $\neq$0 , denormal values are represented.
d) When E′= 2555 and M$\neq$0, the value represented is called Not a number.

17. Write the Add/subtract rule for floating point numbers.

Ans: 1) Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents.

2) Set the exponent of the result equal to the larger exponent.
3) Perform addition/subtraction on the mantissa and determine the sign of the result
4) Normalize the resulting value, if necessary.

18. Write the multiply rule for floating point numbers.
Ans:1) Add the exponent and subtract 127.
2) Multiply the mantissa and determine the sign of the result .
3) Normalize the resulting value , if necessary.

19. What is guard bit?
Ans: Although the mantissa of initial operands are limited to 24 bits, it is important to retain extra bits, called as guard bits.

20. What are the ways to truncate the guard bits?
Ans: There are several ways to truncate the guard bits:
1) Chooping
2) Von Neumann rounding
3) Rounding

21. Define carry save addition(CSA) process.
Ans: Instead of letting the carries ripple along the rows, they can be saved and introduced into the next roe at the correct weighted position. Delay in CSA is less than delay through the ripple carry adder.

22. What are generate and propagate function?
Ans: The generate function is given by

$$G_i = x_i y_i \quad \text{and}$$

The propagate function is given as

$$P_i = x_i + y_i$$

23. What is excess-127 format?
Ans: Instead of the signed exponent E, the value actually stored in the exponent field is and unsigned integer E'

Ans: In some cases, the binary point is variable and is automatically adjusted as computation proceeds. In such case, the binary point is said to float and the numbers are called floating point numbers.

25. In floating point numbers when so you say that an underflow or overflow has occurred?
Ans: In single precision numbers when an exponent is less than -126 then we say that an underflow has occurred. In single precision numbers when an exponent is less than +127 then we say that an overflow has occurred.

UNIT III- BASIC PROCESSING UNIT

1. What are the basic steps required to execute an instruction by the processor?

Ans: The basic steps required to execute an instruction by the processor are:

1) Fetch the contents of the memory location pointed to by the PC. They are loaded into the IR.

$$IR \leftarrow [[PC]]$$

2) Assuming that the memory is byte addressable, increment the contents of the PC by 4, that is

$$PC \leftarrow [PC\} + 4$$

3) Carry out the action specified by the instruction in the IR.

2. Define datapath in the processor unit.

Ans: The registers , The ALU and the interconnecting bus are collectively referred to as the datapath.

3. What is processor clock?

Ans: All operations and data transfers within the processor take place within time periods defined by the processor clock .

4. Write down the control sequence for Move (R1), R2.

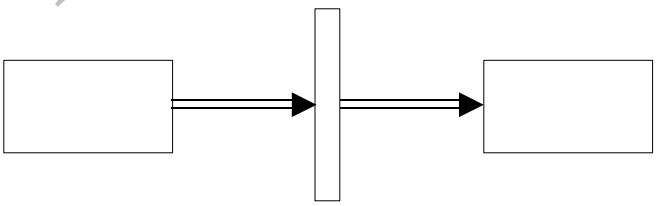
Ans: The control sequence is :

$R1_{out}$, MAR_{in},Read
MDR_{outE},WMFC
MDR_{out},$R2_{in}$

5.Define register file .

Ans: A set of general purpose registers are called as register file Each register from register file R_0 is individually addressable.

6. Draw the hardware organization of two-stage pipeline?



Inter stage buffer

7.What is the role of cache memory in pipeline?

Ans: The use of cache memory is to solve the memory access problem. When cache is included in the processor the access time to the cache is usually the same time needed to perform other basic operation inside the processor.

8.Name the methods for generating the control signals.

Ans: The methods for generating the control signals are:

1) Hardwired control
2) Microprogrammed control

9. Define hardwired control.

Ans: Hard-wired control can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction.

10. Define microprogrammed control.

Ans: A microprogrammed control unit is built around a storage unit is called a control store where all the control signals are stored in a program like format. The control store stores a set of microprograms designed to implement the behavior of the given instruction set.

11. Differentiate Microprogrammed control from hardwired control.

Microprogrammed control	**Hardwired control**
It is the microprogram in control store that generates control signals.	It is the sequential circuit that generates control signals.
Speed of operation is low, because it involves memory access.	Speed of operation is high.
Changes in control behavior can be implemented easily by modifying the microinstruction in the control store.	Changes in control unit behavior can be implemented only by redesigning the entire unit.

12. Define parallelism in microinstruction.

Ans: The ability to represent maximum number of micro operations in a single microinstruction is called parallelism in microinstruction.

13. What are the types of microinstructions available?

Ans: 1) Horizontal microinstruction
2) Vertical microinstruction

Ans:

Horizontal	**Vertical**
Long Formats	Short Formats
Ability to express a high degree of parallelism	Limited ability to express parallel micro operation
Little encoding of control information	Considerable encoding of control information

15. What is MFC?

Ans: To accommodate the variability in response time, the processor waits until it receives an indication that the requested read operation has been completed. This is accomplished by a control signal called Memory – Function – Completed.

16. What are the major characteristics of a pipeline?

Ans: The major characteristics of a pipeline are:

a) Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.

b) The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

c) If the task that can be subdivided has uneven length of execution times, then the speedup of the pipeline is reduced.

d) Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.

17. What is a pipeline hazard?

Ans: Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.

17. What are the types of pipeline hazards?

Ans: The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

18. What is data hazard?

Ans: Any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline is called data hazard.

19. What is Instruction or control hazard?

Ans: The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazard.

20. Define structural hazards.

access to memory.

21. What is side effect?

Ans: When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

22. What do you mean by branch penalty?

Ans: The time lost as a result of a branch instruction is often referred to as branch penalty.

23. What is branch folding?

Ans: When the instruction fetch unit executes the branch instruction concurrently with the execution of the other instruction, then this technique is called branch folding.

24. What do you mean by delayed branching?

Ans: Delayed branching is used to minimize the penalty incurred as a result of conditional branch instruction. The location following the branch instruction is called delay slot. The instructions in the delay slots are always fetched and they are arranged such that they are fully executed whether or not branch is taken. That is branching takes place one instruction later than where the branch instruction appears in the instruction sequence in the memory hence the name delayed branching.

25. What are the two types of branch prediction techniques available?

Ans: The two types of branch prediction techniques are

1) Static branch prediction
2) Dynamic branch prediction

UNIT IV - MEMORY SYSTEM

1. Define Memory Access Time?

Ans: It is the time taken by the memory to supply the contents of a location, from the time, it receives "READ".

2. Define memory cycle time.

Ans: It is defined as the minimum time delay required between the initaiation of two successive memory operations.

3. What is RAM?

This storage location can be accessed in any order and access time is independent of the location being accessed

4. What is cache memory?

5. Explain virtual memory.

Ans: The data is to be stored in physical memory locations that have addresses different from those specified by the program. The memory control circuitry translates the address specified by the program into an address that can be used to access the physical memory.

6. List the various semiconductors RAMs?

i] Static RAM.
ii] Dynamic RAM

7. What do you mean by static memories?
Ans: Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.

8. Define DRAM's.
Ans: Atatic Rams are fast but their cost is high so we use dynamic RAMs which do not retain their state indefinitely but here the information are stored in the form of charge on a capacitor

9. Define DDR SDRAM.
The double data rate SDRAMs are the faster version of SDRAM. It transfers data on both edges of the clock.

10. What is ROM?
ROM is by definition Non Volatile Preprogrammed with information permanently encoded in the chip.

11. What is the mapping procedures adopted in the organization of a Cache Memory?

i) Associative mapping.
ii) Direct mapping.
iii) Set-associative mapping

12. Give the format for main memory address using direct mapping f unction for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.

13. Give the format for main memory address using associative mapping f unction for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.

14. Give the format for main memory address using set associative mapping f unction for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.

15. Define Hit and Miss?

The performance of cache memory is frequently measured in terms of a quantity called hit ratio. When the CPU refers to memory and finds the word in cache, it is said to produce a hit. If the word is not found in cache, then it is in main memory and it counts as a miss.

16. Write the formula for the average access time experienced by the processor in a system with two levels of caches.

Ans: The formula for the average access time experienced by the processor in a system with two levels of caches is

t_{ave}= h1C1+(1-h1)h2C2+(1-h1)(1-h2)M

h1= hit rate in the L1 cache.

h2= hit rate in the L2 cache.

C1=time to access information in the L1 cache.

C2= time to access information in the L1 cache.

M= time to access information in the main memory.

17. What are the enhancements used in the memory management?

Ans: 1) Write Buffer

2) Pre fetching

3) Look- up Cache.

18. What do you mean by memory management unit?

Ans: The memory management unit is a hardware unit which translates virtual addresses into physical addresses in the virtual memory techniques.

19. Explain main (primary) memory.

Ans: This memory stores programs and data that are active in use. Storage locations in main memory are addressed directly by the CPU's load and store instructions.

20. What do you mean by seek time?

Ans: It is the time required to move the read/write head in the proper track.

21. What is disk controller?

rest of the computer system.

22. What is RAID?

Ans: High performance devices tend to be expensive. So we can achieve very high performance at a reasonable cost by using a number of low-cost devices oerating in parallel. This is called RAID(Redundant array of Inexpensive Disks).

23. Define data stripping?

Ans: A single large file is stored in several separate disk units by breaking the file up into a number of smaller pieces and storing these pieces on different disks. This is called data stripping.

24. How the data is organized in the disk?

Ans: Each surface is divided into concentric tracks and each track is divided into sectors. The set of corresponding tracks on all surfaces of a stack of disks forms a logical cylinder. The data are accessed by using read/write head.

25. Define latency time.

Ans: This is the amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head.

UNIT V- I/O ORGANIZATION

1. Why IO devices cannot be directly be connected to the system bus?

Ans: The IO devices cannot be directly connected to the system bus because

i. The data transfer rate of IO devices is slower that of CPU.
ii. The IO devices in computer system has different data formats and work lengths that of CPU.

So it is necessary to use a module between system bus and IO device called IO module or IO system

2. What are the major functions of IO system?

Ans: i. Interface to the CPU and memory through the system bus.
ii. Interface to one or more IO devices by tailored data link.

3. What is an I/O Interface?

Ans: Input-output interface provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices

4. Write the factors considered in designing an I/O subsystem?

Ans:

1. Data Location: Device selection, address of data with in device(track, sector etc)
2. Data transfer: Amount, rate to or from device.
3. Synchronization: Output only when device is ready, input only when

4

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Memory or between an I/O device and CPU.

5. Explain Direct Memory Access.

Ans: A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.

6. Define DMA controller.

Ans: The I/O device interface control circuit that is used for direct memory access is known as DMA controller.

7. What is polling?

Ans: Polling is a scheme or an algorithm to identify the devices interrupting the processor. Polling is employed when multiple devices interrupt the processor through one interrupt pin of the processor**.**

8. What is the need of interrupt controller?

Ans: The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt requests from various devices and allow one by one to the processor.

9. What is a Priority Interrupt?

Ans: A priority interrupt is an interrupt that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously.

10. Define bus.

Ans: When a word of data is transferred between units, all the bits are transferred in parallel over a set of lines called bus. In addition to the lines that carry the data, the bus must have lines for address and control purposes.

11. Define synchronous bus.

Ans: Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.

12. Define asynchronous bus.

Ans: Asynchronous buses are the ones in which each item being transferred is accompanied by a control signal that indicates its presence to the destination unit. The destination can respond with another control signal to acknowledge receipt of the items.

13. What do you mean by memory mapped I/O?

Ans: In Memory mapped I/O, there are no specific input or output instructions. The CPU can manipulate I/O data residing in interface registers with the same instructions that are used to manipulate memory words i.e. the same set of instructions are used for

14. What is program-controlled I/O?

Ans: In program controlled I/O the processor repeatedly checks a status flags to achieve the required synchronization between the processor and an input and output device.

15. Define interrupt.

Ans: An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.

16. Define exception.

Ans: The term exception is used to refer to any event that causes an interruption

17. What are the different methods used for handling the situation when multiple interrupts occurs?

Ans: 1) Vectores interrupts
2) Interrupt nesting
3) Simultaneous Requests.

18. What is a privileged instruction?

Ans: To protect the operating system of a computer from being corrupted by user programs, certain instructions can be executed only while the processor is in the supervisor mode. These are called privileged instruction.

19. What is bus arbitration?

Ans: it is process by which the next device to become the bus master is selected and bus mastership is transferred to it. There are two ways for doing this:

1. Centralized arbitration
2. Distributed arbitration.

20. What is port? What are the types of port available?

Ans: An I/O interface consists of circuitry required to connect an I/O device to computer bus. One side consists of a data path with its associated controls to transfer data between the interface and I/O device. This is called port. It is classified into:

1) Parallel port
2) Serial port.

21. What is a parallel port?

Ans: A parallel port transfers data in the form a number of bits, typically 8 to 16, simultaneously to or from the device.

22. What is a serial port?

Ans: A serial port transfers and receives data one bit at a time.

23. What is PCI bus?

Ans: The Peripheral component interconnect(PCI) bus is a standard that supports the

any particular

processor.

24. What is

SCSI?

Ans: It is the acronym for small computer system interface. It refers to a standard bus defined ANSI. Devices such as disks are connected to a computer via 50-wire cable, which can be upto 25 meters in length and can transfer data at rate up to 55 megabytes/s.

25. Define USB.

Ans: The Universal Serial Bus(USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and easy to use interconnection system.

16 MARKS QUESTIONS WITH HINTS:

1. What are the functional units of a computer? Explain briefly.

Hints: The different functional units are:

1) Input Unit.
2) Output Unit.
3) Memory Unit.
4) Arithmetic & logic Unit.
5) Control Unit.

Refer Page no. 3-7

2. Explain the basic operational concepts of a computer.

Hints: Explain about the MAR, MDR, and the connection between the processor and the memory with a neat diagram.
Refer page no. 7-9.

3. Describe the different classes of instruction format with example and different addressing modes.

Hints: The different instruction formats are :
1) Three address instruction
2) Two address instruction
3) Zero address instruction
Refer page no. 38-42
The different addressing modes are:

- Immediate addressing mode
- Register addressing mode
- Direct or absolute addressing mode
- Indirect addressing mode
- Indexed addressing mode
- Relative addressing mode
- Autoincrement
- Autodecrement

Refer Page no.
48-58.

4. Explain the basic input operations with suitable examples.

Hints: Expalin about program-controlled I/O and memory mapped I/O. Draw the diagram of bus connection for processor , keyboard and display.
Refer Page no. 64-68

5. Write short notes on

i) Software performance

Hints: Refer page no. 10-12.

ii) Memory locations and addresses

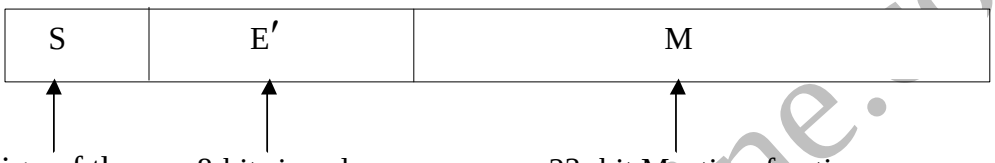
Hints: Explain about byte addressability, big endian and little endian assignments, word alignment. Refer page no. 33-36.

6. Describe the multiplication speed up technique with an example.

Hints: There are two techniques to speed up the multiplication process:
1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands ie bit pair recoding .
2) The second technique reduces the time needed to add the summands i.e Carry save addition
Refer page no. 383-390

7. Explain the floating point Addition – subtraction unit with neat diagram.

Hints: In some cases, the binary point is variable and is automatically adjusted as computation proceeds. In such case, the binary point is said to float and the numbers are called floating point numbers.



Sign of the Number
0 – Positive
1 - Negative

8-bit signed exponent in excess-127 representations

23- bit Mantissa fraction

value represented= $\pm$ 1. M$\times$ 2^{E-127}

1) Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents.
2) Set the exponent of the result equal to the larger exponent.
3) Perform addition/subtraction on the mantissa and determine the sign of the result
4) Normalize the resulting value, if necessary.
Refer page no. 393-402. Draw the diagram.

8. Explain the organization of a sequential binary multiplier with example.

Hints:
procedure.

Draw the diagram. Refer page no. 376-379.

9. Explain the Booth algorithm. Multiply 11$\times$-9 using Booth algorithm

Hints: Explain about the Booth algorithm.The advantages are:
1) It handles both positive and negative multiplier uniformly.
2) It achieves efficiency in the number of additions required when the multiplier has a few large blocks of 1's.
3) The speed gained by skipping 1's depends on the data

10. Explain the Integer division techniques with suitable example.

Hints: The algorithm for restoring division:

Do the following for n times:

1) Shift A and Q left one binary position.
2) Subtract M and A and place the answer back in A.
3) If the sign of A is 1, set q0 to 0 and add M back to A.

Where A- Accumulator, M- Divisor, Q- Dividend

Give an example.

The algorithm for non restoring division:

Do the following for n times:

Step 1: Do the following for n times:

1) If the sign of A is 0 , shift A and Q left one bit position and subtract M from A; otherwise , shift A and Q left and add M to A.
2) Now, if the sign of A is 0,set q0 to 1;otherwise , set q0 to0.

Step 2: if the sign of A is 1, add M to A.

Give an example.

Refer page no. 390-393.

11. Explain the multiple bus organization structure with neat diagram.

Hints: The multiple bus organization is using more buses instead of one bus to reduce the number of steps needed and to provide multiple paths that enable several transfers to take place in parallel.

Refer page no. 423-425.

12. Describe the Hardwired control method for generating the control signals

Hints: Hard-wired control can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction

Refer page no. 425- 429

13.Describe the micro programmed control unit in detail.

Hints: A micro programmed control unit is built around a storage unit is called a control store where all the control signals are stored in a program like format. The control store stores a set of micro programs designed to implement the behavior of the given instruction set.

Refer page no. 429-445

14. Give the organization of the internal data path of a processor that supports a 4-stage pipeline for instructions and uses a 3- bus structure and discuss the same.

Hints: The speed of execution of programs can be improved by arranging the hardware so that more than one operation can be performed at the same time.

Explain about the 4- stage pipeline.

Refer page no. 4556-459

For 3- bus structure refer page no. 479-481.

15. What is pipelining? What are the various hazards encountered in pipelining? Explain in detail.

Hints: The major characteristics of a pipeline are:

a) Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.

b) The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

c) If the task that can be subdivided has uneven length of execution times, then the speedup of the pipeline is reduced.

d) Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.

The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

Refer page no. 459-476.

16. Describe the three mapping techniques used in cache memories with suitable Example.

Hints: The cache memory is a fast memory that is inserted between the larger slower main memory and the processor. It holds the currently active segments of a program and their data.

iii) Associative mapping.
iv) Direct mapping.
iii) Set-associative mapping

Refer page no. 314-325

17. Explain with neat diagram the internal organization of bit cells in a memory chip.

Hints: Memory cells are usually organized in the form of an array, in which each cell is capable of storing one bit of information. Each row consists a memory word, and all cells of a row are connected to a common line referred to as word line, which is driven by he address decoder on the chip.

Refer Page no. 295-297.

Hints:

different from those specified by the program. The memory control circuitry translates the address specified by the program into an address that can be used to access the physical memory.

Refer page no. 337-343

19. Explain the various secondary storage devices in detail.

Hints: The various secondary storage devices are:

1. Magnetic hard disks
2. Optical disks
3. Magnetic tape systems Refer page no. 344-359

20. What is memory interleaving? Explain with neat diagram.

Hints: The main memory of a computer is structure as a collection of physically separate modules each with its own address buffer register and data buffer register, memory access operations may proceed in more than one module at the same time. Thus the aggregate rate of transmission of words to and from the main memory system can be increased.

Refer page no. 330-331

21. Describe the data transfer method using DMA.

Hints: A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.

Refer page no. 234-240.

22. Explain about the interrupts in detail

Hints: An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.

Refer page no. 208-221.

23. Explain the different types of buses with neat diagram.

Hints: When a word of data is transferred between units, all the bits are transferred in parallel over a set of lines called bus. In addition to the lines that carry the data, the bus must have lines for address and control purposes.The different types of buses are:

1. Synchronous Buses:

Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.

2. Asynchronous buses

by a control signal that indicates its presence to the destination unit. The destination can respond with another control signal to acknowledge receipt of the items.

Refer page no. 241-247

24. Explain the various interface circuits.

Hints: An I/O interface consists of circuitry required to connect an I/O device to computer bus. One side consists of a data path with its associated controls to transfer data between the interface and I/O device. This is called port. It is classified into:

1) Parallel port
2) Serial port.
Refer page no. 248-259.

25. Explain in details the various standard I/O interfaces.

Hints: The various standard I/O interfaces are:

1. The Peripheral component interconnect(PCI) bus is a standard that supports the functions found on a processor bus but in a standardized format that is independent of any particular processor
2. It is the acronym for small computer system interface. It refers to a standard bus defined ANSI. Devices such as disks are connected to a computer via 50-wire cable, which can be upto 25 meters in length and can transfer data at rate up to 55 megabytes/s.
3. The Universal Serial Bus(USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and easy to use interconnection system.

Refer Page no. 259-281.